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M68HC05SC family

Technical Summary
8-bit microcontroller family with security features

Members of the M68HC05SC family of single chip MCUs are designed specifically for incorporation into smart card and embedded conditional access applications as well as other security conscious MCU applications. They are based on the industry-standard M68HC05 low power HCMOS core and give full access to its powerful instruction set. Motorola has been the leader in smart card chip technology since the concept was first proposed; the company was the first to support the smart card (as a two chip solution in 1977) and in 1979 developed the first single chip solution. There exists a wide range of potential applications for MCU devices with on-chip security features; current high volume markets include GSM, pay TV and banking. The growth of these new markets has led to the continuing development of Motorola's portfolio of such devices; the company's long association with the field of smart card technology has meant that Motorola now has unrivalled expertise in the design and manufacture of MCUs for security conscious applications. This, combined with an in-depth understanding of current and future markets, has ensured that Motorola's chips are now the standard used by all major smart card manufacturers.

The circuits are designed in accordance with the ISO standard for integrated circuit cards (ISO 7816) and, where appropriate, the GSM SIM specifications 11.10 and 11.11. Three of the family members (the MC68HC05SC21, 'SC27 and 'SC28) are available screened to the requirements of GSM; refer to your Motorola Sales Office for more information. Software and hardware development for all the devices is fully supported by Motorola's range of development systems.

This document contains a description of features common to all members of the M68HC05SC family, with features specific to individual devices noted where appropriate and summarized in Table 1.

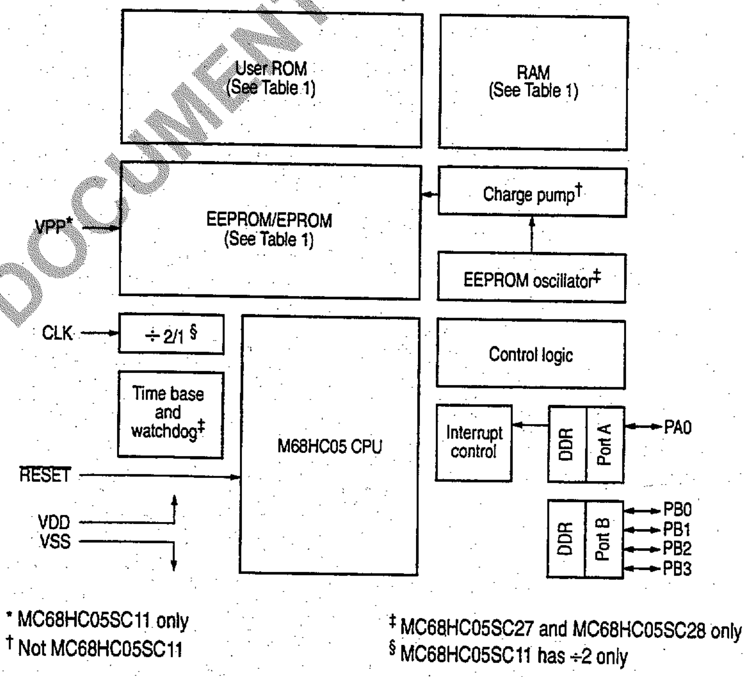


Figure 1 M68HC05SC family block diagram

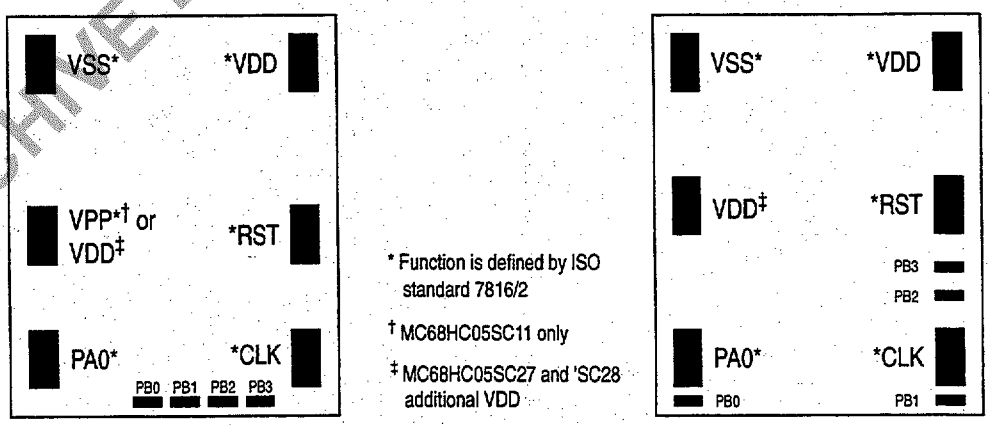
This document contains information on products under development. Motorola reserves the right to change or discontinue these products without notice.

M68HC05SC family features

- HCMOS technology – fully static operation
- 8-bit architecture, based on the industry-standard M68HC05 CPU core
- 2.5 MHz internal operating frequency at 5 MHz clock frequency
- 5 bidirectional I/O lines – ISO standard (ISO 7816/3) I/O port plus an additional 4-bit I/O port
- External maskable interrupt on ISO standard I/O port
- 8 bits x 8 bits unsigned multiply instruction
- Memory mapped I/O
- True bit manipulation
- Security features
- Power-up detection
- Bond pad layout conforms to ISO standard ISO 7816/2
- The MC68HC05SC11, 'SC21, 'SC24 and 'SC27 are available in die-on-wafer form, 16-pin PDIP and 20-pin SOIC packaging, with die packaged in 6- and 8-pin modules available from selected third party suppliers; the MC68HC05SC28 is available in die-on-wafer form and 44-pin PLCC packaging.

Table 1 M68HC05SC family features

Device	Die size	Memory (bytes)				Additional features
		RAM	ROM	EEPROM	EPROM	
MC68HC05SC11	3.5mm x 5.6mm	128	6144	—	8192	• Power saving STOP/WAIT mode
MC68HC05SC21	2.9mm x 5.1 mm	128	6144	3008	—	• On-chip charge pump for EEPROM programming
MC68HC05SC24	2.8mm x 3.7mm	128	3072	1040	—	• Power saving STOP and WAIT modes • 4MHz internal operating frequency with divide by one clock option (refer to Sales Office)
MC68HC05SC27	4.2mm x 5.0mm	240	16384	3008	—	• 3 – 5.5V operation • On-chip charge pump for EEPROM programming driven by independent internal oscillator • Power saving STOP and WAIT modes
MC68HC05SC28	4.9mm x 5.3mm	240	12800	8112	—	• Time base circuitry with maskable interrupt capability driven from either a free-running oscillator or an external clock source • Watchdog capability under software control • 4MHz internal operating frequency with divide by one clock option (refer to Sales Office)



MC68HC05SC11, 'SC21, 'SC24 and SC27

MC68HC05SC28

Figure 2 M68HC05SC family bond pad layouts

Functional pin description

VDD and VSS

Power is supplied to the microcontroller via these pins. VDD is the positive supply and VSS is ground.

It is in the nature of CMOS designs that very fast signal transitions occur on the MCU pins. These short rise and fall times place very high short-duration current demands on the power supply. To prevent noise problems, special care must be taken to provide good power supply bypassing at the MCU. Bypass capacitors should have good high-frequency characteristics and be as close to the MCU as possible. Bypassing requirements vary, depending on how heavily the MCU pins are loaded.

RESET

This active low input pin has an internal pull-up resistor and is used to reset the MCU. Applying a logic zero to this pin forces the device to a known start-up state.

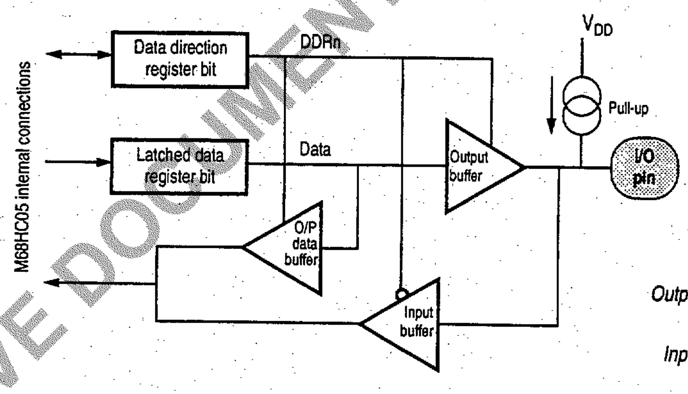
CLK

The CLK pin provides the chip with an external clock signal which is divided by two to generate the internal clocks. A divide by one clock option is also available on all devices except the MC68HC05SC11.

PA0 and PB0–PB3

These 5 lines comprise the 1-bit port A and the 4-bit port B. The bidirectional port lines may be programmed as inputs or outputs under software control. The direction of each pin is determined by the state of the corresponding bit in the port data direction register (DDR). Each port has an associated DDR. Any I/O port pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero.

At power-on or reset, all DDRs are cleared, thus configuring all port pins as inputs. The data direction registers can be written to, or read by, the MCU. During the programmed output state, a read of the data register actually reads the value of the output data latch and not the I/O pin. The operation of the port hardware is shown schematically in Figure 3.



	DDRn	Data	I/O pin
Output	1	0	0
	1	1	1
Input	0	0	tristate
	0	1	tristate

Figure 3 Standard I/O port structure

VPP — MC68HC05SC11 only

When programming, VPP is used to provide the high voltage to the EPROM. When reading the EPROM, VPP may go to a higher voltage than that on VDD without affecting the read operation. VPP may be lower than VDD during the power-on sequence, but must be forced to VDD during long term operation for reliability reasons.

The rate of change of voltage on VPP must not exceed 2V μs^{-1}.

Memory and registers

Figure 4 shows the memory map of the M68HC05SC family; RAM, ROM and non-volatile memory sizes are given in Table 2.

Note: The state of the data bus during a read of unused locations is undefined.

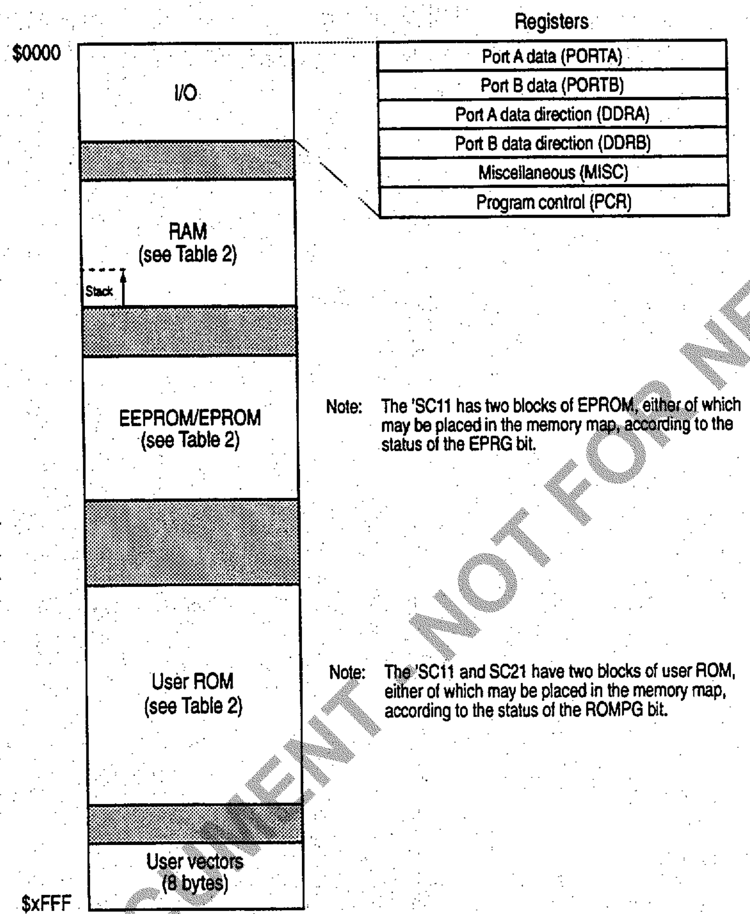


Figure 4 Memory map of the M68HC05SC family

RAM

See Table 2 for a summary of the amount of RAM on each device. The top 64 bytes of RAM are shared with the stack area. The stack is used to store the return address for subroutine calls and the machine state during interrupts. After reset the stack starts at the highest location. These 64 bytes can be used for data, but care must be taken to ensure that they are not corrupted by stacking.

ROM

The MC68HC05SC11 and 'SC21 have ROM on two pages (PAGE0 and PAGE1); paging is controlled by the ROMPG bit. In both devices, PAGE0 contains 3840 bytes and holds the reset and interrupt vectors in its eight highest locations. PAGE1 is accessed by setting ROMPG; only the lowest 2304 bytes are different from PAGE0. It is recommended that the interrupt service routine is placed in the area of ROM that is common to both PAGE0 and PAGE1.

Table 2 Memory format

Device	Memory (bytes)			
	RAM	ROM	EEPROM	EPROM
MC68HC05SC11	128	PAGE0 (ROMPG = 0): 3840 PAGE1 (ROMPG = 1): 2304	—	PAGE0 (EPRPG = 0): 4096 PAGE1 (EPRPG = 1): 4096
MC68HC05SC21	128	PAGE0 (ROMPG = 0): 3840 PAGE1 (ROMPG = 1): 2304	3008	—
MC68HC05SC24	128	3072	1040	—
MC68HC05SC27	240	16384	3008	—
MC68HC05SC28	240	12800	8112	—

The MC68HC05SC24, 'SC27 and 'SC28 each has a single page of user ROM. The reset and interrupt vectors occupy the eight highest bytes in this ROM block.

EPROM/EEPROM

The MC68HC05SC11 has 8192 bytes of EPROM mapped on two pages (PAGE0 and PAGE1) under control of the EPRPG bit. Each page contains 4096 bytes of EPROM. The two modes of operation of the EPROM are the read mode and the write mode.

The MC68HC05SC21 and 'SC27 have 3008 bytes of user EEPROM, the 'SC24 has 1040 bytes of user EEPROM and the 'SC28 has 8112 bytes of user EEPROM. The two modes of operation of the EEPROM are the read mode and the programming mode. The programming mode can be either a write mode or an erase mode.

NVM programming

Programming circuitry embedded in the NVM block allows a group of up to four bytes to be erased (EEPROM only) or written simultaneously. A write instruction can be used to program individual bits of the defined word, while an erase instruction forces zeros in all bits of the defined word. In the MC68HC05SC11, 'SC21 and the 'SC24, the four bytes are those whose addresses share the same eleven most significant bits out of the thirteen used to define a word. In the MC68HC05SC27 and 'SC28, the four bytes are those whose addresses share the same thirteen most significant bits out of the fifteen used to define a word.

NVM write operation

As described above, up to four different bytes can be written simultaneously. When writing the first of these four bytes, the NVM address bits of the word are captured in the address register and the corresponding data is stored in one of the four NVM data registers as selected by the two least significant bits of the address. The other three bytes of the word can be stored in the three other unused data registers by issuing three other writes into the corresponding NVM locations. Only when VPP is applied (EPROM) or the charge pump is activated (EEPROM) are the contents of the four NVM data registers programmed simultaneously into the NVM array locations.

NVM characteristics

(V_{DD} = 5.0 Vdc ± 10%, T_A = −30 to +70°C)

EPROM programming time, t_{PROG} (minimum)(1)	5 ms
EEPROM programming/erase time, t_{PROG} (minimum)(2)	10 ms
Write/erase endurance(2)(3)	10,000 cycles
Data retention(3)	10 years

(1) MC68HC05SC11 only

(2) All devices except MC68HC05SC11

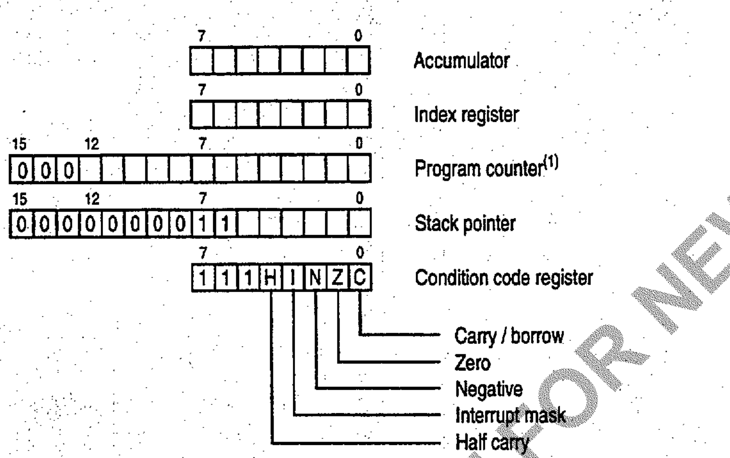
(3) These parameters are temperature dependent and are quoted for the worst case (70°C). Better performance will usually be obtained for operation at normal temperatures. Refer also to Motorola's current ***Reliability Report*** for up-to date failure rate information.

I/O registers

The I/O ports A and B with their associated DDR registers are located in the first bytes of memory, as shown in Figure 4.

CPU registers

The MCU contains five registers, as shown in the programming model of Figure 5.



(1) In the MC68HC05SC11, 'SC21 and 'SC24 program counters, bits 15 to 13 are permanently fixed at zero, while in the MC68HC05SC27 and 'SC28 program counters, only bit 15 is permanently fixed at zero.

Figure 5 Programming model

Accumulator (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

Index register (X)

The index register contains the indexed addressing value used to create an effective address, and may also be used as a temporary storage area.

Program counter (PC)

The program counter is a register containing the address of the next byte to be fetched

Stack pointer (SP)

The stack pointer is a register containing the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to its highest location. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and overwrites the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.

Condition code register (CCR)

The CCR is a register in which four bits are used to indicate the results of the instruction just executed, and the fifth bit indicates whether interrupts are masked. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

- Half carry (H) — This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.
- Interrupt (I) — When this bit is set all maskable interrupts are masked. If an interrupt occurs while this bit is set, the interrupt is latched and remains pending until the interrupt bit is cleared.
- Negative (N) — When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative.
- Zero (Z) — When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.
- Carry/borrow (C) — When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during 'bit test and branch' instructions and during shifts and rotates.

Resets

The active low $\overline{\text{RESET}}$ input pin forces the chip to a known internal state and provides an orderly software start-up procedure.

Even if the $\overline{\text{RESET}}$ pin is not held low during power-up, the power-up detection circuitry will trigger an internal reset of the device when the supply voltage is applied to VDD.

On the MC68HC05SC7 and 'SC28, a reset may also be initiated by software.

Interrupts

Microprocessor based systems may require that normal processing be interrupted so that external events may be serviced; polling for asynchronous events (i.e. 'interrupts') can be done by dedicated hardware. Background tasks, then, do not have to be suspended during polling; they will be interrupted only when necessary. Each device can be interrupted either by a hardware interrupt on PA0, or by a non-maskable software interrupt (SWI) which is executed regardless of the I-bit value. If both a maskable hardware interrupt and SWI occur at the same time then SWI is executed first. The MC68HC05SC27 and 'SC28 can also be interrupted by a time base interrupt.

When an interrupt is serviced, normal processing is suspended at the end of the current instruction execution. The processor registers are then saved on the stack and the interrupt mask bit I is set to prevent additional interrupts from being serviced. The appropriate interrupt vector then points to the starting address of the interrupt service routine. Upon completion of that routine, the RTI instruction (which is usually part of the interrupt service routine) causes the processor registers' contents to be recovered from the stack before returning to normal processing; in particular, the I-bit is cleared.

Hardware interrupt

If enabled, a negative transition on PA0 latches an interrupt request, and sets the INTFF flip-flop. Once set, this bit blocks any subsequent negative edges on PA0 affecting the interrupt request latch. The interrupt request will be either processed if the I-bit is already cleared, or will be pending until the I-bit is cleared.

When set, INTFF acts as a general interrupt mask in addition to the I-bit. To allow further interrupts to be processed, INTFF must be cleared by software. Prior to an I/O activity on PA0, INTFF may need to be set, otherwise an unwanted interrupt will be latched which can only be cancelled by servicing a dummy interrupt routine.

Software interrupt

Software interrupt (SWI) is an instruction that is executed regardless of the state of the interrupt mask bit I.

Time base interrupt — MC68HC05SC27 and MC68HC05SC28 only

If enabled, a time base interrupt is generated on each time base timeout.

Low power modes

During WAIT mode, power consumption is reduced by switching off the processor clocks, thereby suspending the operation of the processor. All on-board functions that are capable of generating interrupt requests, e.g. timers, continue to run as normal. The device can be brought out of WAIT mode by a system reset, an external interrupt on the PA0 pin or, in the case of the MC68HC05SC27 and 'SC28, an internal interrupt generated by the time base function.

STOP mode is the lowest power consumption mode. All on-board clocks are stopped, thereby switching off the processor and all the on-board functions. The device can be brought out of STOP mode by a system reset or by an external interrupt on the PA0 pin.

The MC68HC05SC11 supports only one low power mode; this is known as STOP/WAIT mode and is equivalent to the WAIT mode described above. The other devices covered by this document support both STOP and WAIT modes.

Time base — MC68HC05SC27 and MC68HC05SC28 only

The time base is a 13-bit up-counter which can either increment at the processor clock rate or at a rate determined by an independent internal free-running oscillator. Every time the counter rolls over (from $1FFF to 0000), an overflow signal is generated which can be used to generate an interrupt request.

Watchdog system — MC68HC05SC27 and MC68HC05SC28 only

When enabled, the software controlled watchdog system uses the time base to trigger an internal reset of the device. If the watchdog counter reaches its largest value after a time base timeout, then a watchdog reset will be activated. This feature is intended to detect program runaway, and to force resumption of the correct program flow.

Security features

Members of the M68HC05SC family of MCUs with on-chip security features have been designed and manufactured with the needs of security conscious applications in mind. The design of the devices includes features that make the unauthorized access of the on-chip memory more difficult. Manufacturing occurs in a controlled environment and is strictly monitored; wafers are accounted for; die are tested in a restricted area to ensure the integrity of the product shipped to the customer; even the reject wafers are accounted for and destroyed on-site. Customer defined security data can be programmed into the EPROM/EEPROM on each die during test.

Electrical specifications

Stresses in excess of those listed in Table 3 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect reliability, including NVM data retention and write/erase endurance (see NVM characteristics table on page 5).

Note: For specifications relating to GSM applications, refer to your Motorola Sales Office.

Table 3 Absolute maximum ratings for the device family

Parameter	Symbol	Maximum rating	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage on pins	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating temperature	T_A	T_L to T_H –30 to +70	°C
Storage temperature	T_S	–55 to +125	°C

Table 4 AC electrical characteristics for the MC68HC05SC11

(V_{DD} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = 0°C to T_H, unless otherwise indicated)

Characteristic	Symbol	Min.	Max.	Unit
Frequency of operation: External clock frequency MCU bus frequency	 f_{OSC} f_{OP}	 dc dc	 5.0 2.5	 MHz MHz
Processor cycle time	t_{CYC}	400	—	ns
External clock duty cycle	R_{CLK}	40	60	%
$\overline{RESET}$ pulse width	t_{RL}	2	—	t_{CYC}
Power-on reset delay	t_{PORL}	32	—	t_{CYC}
External clock rise/fall time	t_R, t_F	—	1000	ns

Table 5 DC electrical characteristics for 5V operation for the MC68HC05SC11

(V_{DD} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = 0°C to T_H)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Output high voltage (I_{LOAD} = −0.1 mA)	V_{OH}	$0.7V_{DD}$	—	—	V
Output low voltage (I_{LOAD} = +1.6 mA)	V_{OL}	—	—	0.4	V
Input high voltage Ports, CLK $\overline{RESET}$	V_{IH}	 $0.7V_{DD}$ $V_{DD} - 0.7$	 — —	 $V_{DD} + 0.3$ $V_{DD} + 0.3$	V
Input low voltage Ports, CLK $\overline{RESET}$	V_{IL}	 $V_{SS} - 0.3$ $V_{SS} - 0.3$	 — —	 0.8 0.6	V
Input current ($V_{IH} = V_{DD}$) Ports, CLK, $\overline{RESET}$	I_{IH}	—	—	+ 10	µA
Input current ($V_{IL} = V_{SS}$) Ports, CLK, $\overline{RESET}$	I_{IL}	− 10	—	—	µA
Supply current(1) RUN STOP/WAIT (2)	I_{DD}	 — —	 2.5 250	 4.5 450	 mA µA
Programming current	I_{PP}	—	4n(3)	20	mA
Programming voltage	V_{PP}	14.4	15	15.6	V

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs.
External clock frequency 5 MHz, internal operating frequency 2.5 MHz.

(2) No DC loads, all inputs at V_{DD}.

(3) where n is the number of bytes programmed simultaneously.

Table 6 AC electrical characteristics for the MC68HC05SC21

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise indicated)

Characteristic	Symbol	Min.	Max.	Unit
Frequency of operation:				
External clock frequency	f_{OSC}	0	5.0	MHz
MCU bus frequency (divide by two option)	f_{OP}	0	2.5	MHz
MCU bus frequency (divide by one option)	f_{OP}	0	4.0	MHz
Processor cycle time	t_{CYC}	400	—	ns
Interrupt pulse width	t_{ILIH}	1.5	—	t_{CYC}
External clock duty cycle	R_{CLK}	40	60	%
$\overline{RESET}$ pulse width	t_{RL}	2	—	t_{CYC}
Power-on reset delay	t_{PORL}	32	—	t_{CYC}
External clock rise/fall time	t_R, t_F	—	1000	ns
Input hold time – ports	t_{HOLD}	2	—	t_{CYC}

Table 7 DC electrical characteristics for 5V operation for the MC68HC05SC21

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Output high voltage (I_{LOAD} = –0.1 mA)	V_{OH}	0.7V_{DD}	—	—	V
Output low voltage (I_{LOAD} = +1.6 mA)	V_{OL}	—	—	0.4	V
Input high voltage	V_{IH}				V
Ports, CLK		0.7V_{DD}	—	V_{DD} + 0.3	
$\overline{RESET}$		V_{DD} – 0.7	—	V_{DD} + 0.3	
Input low voltage	V_{IL}				V
Ports, CLK		V_{SS} – 0.3	—	0.8	
$\overline{RESET}$		V_{SS} – 0.3	—	0.6	
Input current ($V_{IH} = V_{DD}$) Ports, CLK, $\overline{RESET}$	I_{IH}	—	—	+ 10	µA
Input current ($V_{IL} = V_{SS}$) Ports, CLK, $\overline{RESET}$	I_{IL}	– 10	—	—	µA
Supply current(1)	I_{DD}				
RUN		—	1.2	TBD	mA
WAIT(2) (no programming)		—	330	TBD	µA
STOP(2)		—	41	TBD	µA
STOP(2) (no external clock)		—	60	TBD	nA

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs.
External clock frequency 5MHz, internal operating frequency 2.5MHz.

(2) No DC loads, all inputs at V_{DD}.

Table 8 AC electrical characteristics for the MC68HC05SC24

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise indicated)

Characteristic	Symbol	Min.	Max.	Unit
Frequency of operation:				
External clock frequency	f_{OSC}	0	5.0	MHz
MCU bus frequency (divide by two option)	f_{OP}	0	2.5	MHz
MCU bus frequency (divide by one option)	f_{OP}	0	4.0	MHz
Processor cycle time	t_{CYC}	400	—	ns
Interrupt pulse width	t_{ILIH}	1.5	—	t_{CYC}
External clock duty cycle	R_{CLK}	40	60	%
$\overline{RESET}$ pulse width	t_{RL}	2	—	t_{CYC}
Power-on reset delay	t_{PORL}	32	—	t_{CYC}
External clock rise/fall time	t_R, t_F	—	1000	ns
Input hold time – ports	t_{HOLD}	2	—	t_{CYC}

Table 9 DC electrical characteristics for 5V operation for the MC68HC05SC24

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Output high voltage (I_{LOAD} = –0.1 mA)	V_{OH}	$0.7V_{DD}$	—	—	V
Output low voltage (I_{LOAD} = +1.6 mA)	V_{OL}	—	—	0.4	V
Input high voltage	V_{IH}				V
Ports, CLK		$0.7V_{DD}$	—	$V_{DD} + 0.3$	
$\overline{RESET}$		$V_{DD} - 0.7$	—	$V_{DD} + 0.3$	
Input low voltage	V_{IL}				V
Ports, CLK		$V_{SS} - 0.3$	—	0.8	
$\overline{RESET}$		$V_{SS} - 0.3$	—	0.6	
Input current ($V_{IH} = V_{DD}$) Ports, CLK, $\overline{RESET}$	I_{IH}	—	—	+ 10	µA
Input current ($V_{IL} = V_{SS}$) Ports, CLK, $\overline{RESET}$	I_{IL}	– 10	—	—	µA
Supply current(1)	I_{DD}				
RUN		—	2.5	5	mA
WAIT(2)(no programming)		—	300	450	µA
STOP(2)		—	200	300	µA
STOP(2)(no external clock)		—	0.5	TBD	µA

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs.
External clock frequency 5MHz, internal operating frequency 2.5MHz.

(2) No DC loads, all inputs at V_{DD}.

Table 10 AC electrical characteristics for the MC68HC05SC27

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise indicated)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation:				
External clock frequency	f_{OSC}	0	5.0	MHz
MCU bus frequency (divide by two option)	f_{OP}	0	2.5	MHz
MCU bus frequency (divide by one option)	f_{OP}	0	4.0	MHz
Processor cycle time	t_{CYC}	400	—	ns
External interrupt pulse width	IT_{LOW}	125	—	ns
External clock duty cycle	R_{CLK}	40	60	%
$\overline{RESET}$ pulse width	t_{RL}	2	—	t_{CYC}
Power-on reset delay	t_{PORL}	32	—	t_{CYC}
External clock rise/fall time	t_R, t_F	—	1000	ns
Time base output frequency (from internal oscillator)	f_{TB}	0.1	0.5	kHz
Input hold time – Ports	t_{HOLD}	2	—	t_{CYC}

Table 11 DC electrical characteristics for 5V operation for the MC68HC05SC27

(V_{DD} = 5.0Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Output high voltage (I_{LOAD} = −0.1 mA)	V_{OH}	$0.7V_{DD}$	—	—	V
Output low voltage (I_{LOAD} = +1.6 mA)	V_{OL}	—	—	0.4	V
Input high voltage	V_{IH}				V
Ports, CLK		$0.7V_{DD}$	—	$V_{DD} + 0.3$	
$\overline{RESET}$		$V_{DD} - 0.7$	—	$V_{DD} + 0.3$	
Input low voltage	V_{IL}				V
Ports, CLK		$V_{SS} - 0.3$	—	0.8	
$\overline{RESET}$		$V_{SS} - 0.3$	—	0.6	
Input current ($V_{IH} = V_{DD}$) Ports, CLK, $\overline{RESET}$	I_{IH}	—	—	+ 50	µA
Input current ($V_{IL} = V_{SS}$) Ports, CLK, $\overline{RESET}$	I_{IL}	- 50	—	—	µA
Supply current(1)	I_{DD}				
RUN		—	5	TBD	mA
WAIT (2) (no programming)		—	0.9	TBD	mA
STOP(2)		—	360	TBD(3)	µA
STOP(2)(no external clock)		—	50	TBD	µA

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs.
External clock frequency 5MHz, internal operating frequency 2.5MHz.

(2) No DC loads, all inputs at V_{DD}.

(3) If the external clock frequency is limited to 1MHz, STOP I_{DD} will not exceed 200µA at 25°C.

Table 12 AC electrical characteristics for the MC68HC05SC28

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise indicated)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation: External clock frequency MCU bus frequency (divide by two option) MCU bus frequency (divide by one option)	 f_{OSC} f_{OP} f_{OP}	 0 0 0	 5.0 2.5 4.0	 MHz MHz MHz
Processor cycle time	t_{CYC}	400	—	ns
External interrupt pulse width	IT_{LOW}	125	—	ns
External clock duty cycle	R_{CLK}	40	60	%
$\overline{\text{RESET}}$ pulse width	t_{RL}	2	—	t_{CYC}
Power-on reset delay	t_{PORL}	32	—	t_{CYC}
External clock rise/fall time	t_R, t_F	—	1000	ns
Time base output frequency (from internal oscillator)	f_{TB}	0.2	0.8	kHz
Input hold time – Ports	t_{HOLD}	2	—	t_{CYC}

Table 13 DC electrical characteristics for 5V operation for the MC68HC05SC28

(V_{DD} = 5.0Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Output high voltage (I_{LOAD} = –0.1 mA)	V_{OH}	0.7V_{DD}	—	—	V
Output low voltage (I_{LOAD} = +1.6 mA)	V_{OL}	—	—	0.4	V
Input high voltage Ports, CLK $\overline{\text{RESET}}$	V_{IH}	 0.7V_{DD} V_{DD} – 0.7	 — —	 V_{DD} + 0.3 V_{DD} + 0.3	V
Input low voltage Ports, CLK $\overline{\text{RESET}}$	V_{IL}	 V_{SS} – 0.3 V_{SS} – 0.3	 — —	 0.8 0.6	V
Input current ($V_{IH} = V_{DD}$) Ports, CLK, $\overline{\text{RESET}}$	I_{IH}	—	—	+ 50	µA
Input current ($V_{IL} = V_{SS}$) Ports, CLK, $\overline{\text{RESET}}$	I_{IL}	– 50	—	—	µA
Supply current(1) RUN WAIT (2) (no programming) STOP(2) STOP(2)(no external clock)	I_{DD}	 — — — —	 5 TBD TBD 50	 TBD TBD TBD(3) TBD	 mA mA µA µA

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs.
External clock frequency 5 MHz, internal operating frequency 2.5 MHz.

(2) No DC loads, all inputs at V_{DD}.

(3) If the external clock frequency is limited to 1 MHz, STOP I_{DD} will not exceed 200µA at 25°C.

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